

Notice of Allowability	Application No.	Applicant(s)	
	09/579,402	KO, KEI-YU	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to 10/21/04.
2. The allowed claim(s) is/are 1-9 and 11-30.
3. The drawings filed on 19 April 2001 are accepted by the Examiner.
4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some*
 - c) None
 of the:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. Notice of References Cited (PTO-892)
2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. Notice of Informal Patent Application (PTO-152)
6. Interview Summary (PTO-413),
Paper No./Mail Date _____
7. Examiner's Amendment/Comment
8. Examiner's Statement of Reasons for Allowance
9. Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1 thru 9, and 11 thru 30 are allowed. The following is an examiner's statement of reasons for allowance: The references of record, either singularly or in combination, do not teach or suggest at least "a gate stack structure situated over a semiconductor material layer, said gate stack structure comprising: a contact plug having a base in contact with said semiconductor material layer, said contact plug comprising a second conductive material, said contact plug having a top and a lateral wall, wherein the second conductive material physically contacts the semiconductor material layer; wherein a conductive layer is disposed along said lateral wall along the second conductive material and with said second conductive material comprises a part of said contact plug" (claims 1-8, 21, and 22).

Regarding claims 9, 23, and 24, the references of record, either singularly or in combination, do not teach or suggest at least "a gate stack structure situated over a monocrystalline silicon layer, said gate stack structure comprising: a contact plug having a base in contact with said semiconductor material layer, said contact plug comprising a second conductive material, said contact plug having a top and a lateral wall, wherein the second conductive material physically contacts the semiconductor material layer; wherein a conductive layer is disposed along said lateral wall along the second conductive material and with said second conductive material comprises a part of said contact plug."

Regarding claims 11-18, 25, and 26, the references of record, either singularly or in combination, do not teach or suggest at least "a gate structure comprising: a pair of gate stacks situated over a semiconductor material layer, each said gate stack comprising: a contact plug

having a base in contact with said semiconductor material layer, said contact plug comprising a second conductive material, said contact plug having a top and a lateral wall, wherein the second conductive material physically contacts the semiconductor material layer; wherein a conductive layer is disposed along said lateral wall along the second conductive material and with said second conductive material comprises a part of said contact plug.”

Regarding claims 19, 27, and 28, the references of record, either singularly or in combination, do not teach or suggest at least “a gate stack structure comprising: a pair of gate stacks situated over a monocrystalline silicon layer, each said gate stack comprising: a contact plug having a base in contact with said monocrystalline silicon layer, said contact plug comprising a second conductive material, said contact plug having a top and a lateral wall, wherein the second conductive material physically contacts the semiconductor material layer; wherein a conductive layer is disposed along said lateral wall along the second conductive material and with said second conductive material comprises a part of said contact plug.”

Regarding claims 20, 29, and 30, the references of record, either singularly or in combination, do not teach or suggest at least “a gate structure comprising: a pair of gate stacks situated over a monocrystalline silicon layer, each said gate stack comprising: a contact plug having a base in contact with said monocrystalline silicon layer, said contact plug comprising a second conductive material, said contact plug having a top and a lateral wall, wherein the second conductive material physically contacts the semiconductor material layer; wherein a conductive layer is disposed along said lateral wall along the second conductive material and with said second conductive material comprises a part of said contact plug.”

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
January 18, 2005


GEORGE ECKERT
PRIMARY EXAMINER